What is Claimed is:

- 1 1. A circuit for generating aligned clock and data signals, comprising:
- 2 a clock input;
- a first circuit path receiving an external clock signal from said clock input, and
- 4 generating an aligned clock signal; and
- 5 a second circuit path generating an aligned data signal;
- 6 wherein said first and second circuit paths comprise identical circuit components.
- 1 2. The circuit as claimed in claim 1, wherein said first and second circuit paths each
- 2 comprises a D flip-flop and an output buffer.
- 1. 3. The circuit as claimed in claim 2, further comprising a clock multiplication circuit for
- 2 receiving said external clock signal and sending a multiplied clock signal to said D
- 3 flip-flops in said first and second circuit paths.
- 1 4. The circuit as claimed in claim 3, wherein said clock multiplication circuit comprises
- 2 a clock multiplier and an inverter.
- 1 5. A circuit for generating aligned clock and data signals, comprising:
- 2 a clock input;
- an inverter receiving an external clock signal from said clock input and generating an
- 4 inverted clock signal;
- a first circuit path receiving said inverted clock signal from said inverter, and
- 6 generating an aligned clock signal; and
- 7 a second circuit path generating an aligned data signal;
- 8 wherein said first and second circuit paths comprise identical circuit components.

- 1 6. The circuit as claimed in claim 5, wherein said first and second circuit paths each
- 2 comprises a D flip-flop and an output buffer.
- 1 7. The circuit as claimed in claim 6, further comprising a clock multiplier receiving said
- 2 external clock signal and sending a multiplied clock signal to said D flip-flop in said
- 3 second circuit path, and an inverter receiving said multiplied clock signal and sending
- an inverted multiplied clock signal to said D flip-flop in said first circuit path.
- 1 8. A circuit for generating aligned clock and data signals, comprising:
- 2 a clock input;
- an inverter receiving an external clock signal from said clock input and generating an
- 4 inverted clock signal,
- 5 a first circuit path receiving said inverted clock signal from said inverter, and
- 6 generating an aligned clock signal;
- 7 a second circuit path generating an aligned data strobe signal;
- 8 a third circuit path generating an aligned first data signal; and
- 9 a fourth circuit path generating an aligned second data signal;
- wherein said first, second, third and fourth circuit paths comprise identical circuit
- 11 components.
- 1 9. The circuit as claimed in claim 8, wherein said first, second, third and fourth circuit
- 2 paths each comprises a D flip-flop and an output buffer.
- 1 10. The circuit as claimed in claim 9, further comprising a clock multiplication circuit
- 2 receiving said external clock signal, sending a multiplied clock signal to said D flip-
- flops in said third and fourth circuit paths, and sending an inverted multiplied clock

- signal to said D flip-flops in said first and second circuit paths.
- 1 11. The circuit as claimed in claim 10, said clock multiplication circuit comprising a
- 2 clock multiplier receiving said external clock signal and sending a multiplied clock
- 3 signal to said D flip-flops in said third and fourth circuit paths, an inverter receiving
- 4 said multiplied clock signal and sending an inverted multiplied clock signal to said D
- 5 flip-flop in said first circuit path, and an inverter receiving said multiplied clock
- 6 signal and sending an inverted multiplied clock signal to said D flip-flop in said
- 7 second circuit path.